

Amendment under article 34

1. (Amended) An impurity introducing method which comprising:
a step of introducing an impurity selected from a group
consisting of B, As, P, Sb and In into a surface of a
5 semiconductor substrate; and
a step of radiating inactive plasma to the surface of the
semiconductor substrate after the impurity introducing step.
2. (Amended) The impurity introducing method according to claim
10 1, wherein the step of radiating the plasma includes a step of
radiating plasma such that the impurity possesses a desired
impurity profile in the semiconductor substrate.
3. (Amended) The impurity introducing method according to claim
15 1 or 2, wherein the step of radiating the plasma includes a step
of radiating plasma which contains at least one kind of rare
gas element.
4. (Amended) The impurity introducing method according to claim
20 3, wherein the step of radiating the plasma includes a step of
radiating He plasma.
5. (Amended) The impurity introducing method according to claim
25 1 or 2, wherein the step of radiating the plasma includes a step
of radiating plasma which contains hydrogen.
6. (Amended) The impurity introducing method according to any

one of claims 1 to 5, wherein the step of introducing the impurity includes a plasma doping step.

5 7. (Amended) The impurity introducing method according to any one of claims 1 to 5, wherein the step of introducing the impurity includes an ion implanting step.

10 8. (Amended) The impurity introducing method according to any one of claims 1 to 5, wherein the step of introducing the impurity includes a gas doping step.

15 9. (Amended) The impurity introducing method according to any one of claims 1 to 8, wherein the semiconductor device is formed to have the impurity profile in which the impurity concentration at a depth position of 4nm is set to 1/10 or more of the impurity concentration on the surface of the semiconductor device.

20 10. (Amended) The semiconductor device according to claim 9, wherein the semiconductor device is formed to have the impurity profile in which the impurity concentration at a depth position of 7nm is set to 1/100 or more of the impurity concentration on the surface of the semiconductor device.

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25 [12] (Deleted)

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